I CLAIM:

1. A semiconductor body having at least one integrated circuit formed at a surface thereof, the at least one integrated circuit comprising:

core functional logic;

a terminal buffer coupled in a signal path between the core functional logic and a terminal pad, for forwarding a signal along the signal path;

a load test switch for selectively connecting a load terminal to the terminal pad;

a first test switch for selectively connecting an input of the terminal buffer to a first test terminal;

a second test switch for selectively connecting an output of the terminal buffer to a second test terminal; and

control circuitry for controlling the operation of the load test switch and the first and second test switches so as to be open in normal operation, and so as to be selectively closed in a test mode.

2. The semiconductor body of claim 1, wherein the at least one integrated circuit further comprises:

an electrostatic discharge protection circuit, connected in the signal path between the terminal pad and the terminal buffer, at a location in the signal path between the load test switch and the terminal buffer.

3. The semiconductor body of claim 1, further comprising:

a bus holder circuit connected to the terminal pad at a node that is between the terminal pad and the terminal buffer.

4. The semiconductor body of claim 1, wherein the terminal buffer comprises an output buffer, the output buffer having an input coupled to the core functional logic and having an output coupled to the terminal pad

and further comprising:

an isolation test switch, for selectively connecting the terminal buffer to the core functional logic;

wherein the control circuitry is also for controlling the operation of the isolation test switch so as to be closed in normal operation, and so as to be open in the test mode.

5. The semiconductor body of claim 4, further comprising:

an input buffer, having an input coupled to the terminal pad and having an output coupled to the core functional logic;

a third test switch for selectively connecting the output of the input buffer to the first test terminal;

wherein the control circuitry is also for controlling the operation of the third test switch so as to be open in normal operation, and so as to be selectively closed in the test mode.

6. The semiconductor body of claim 1, wherein a plurality of integrated circuits are formed at a surface thereof;

wherein the load terminals of the plurality of integrated circuits are connected in common;

wherein the first test terminals of the plurality of integrated circuits are connected in common;

and wherein the second test terminals of the plurality of integrated circuits are connected in common.

7. The semiconductor body of claim 1, wherein the at least one integrated circuit comprises a plurality of terminal buffers, each associated with first and second test switches and load test switches, the first test switches associated with the plurality of terminal buffers connected to a common first test node, the second test switches associated with the plurality of terminal buffers connected to a common second test node, and the load test switches associated with the plurality of terminal buffers connected to a common load node;

and further comprising:

first, second, and third pad switches, connected in series between the first common test node and the first test terminal, the second common test node and the second test terminal, and the common load node and the load terminal, respectively;

wherein the control circuitry is also for controlling the operation of the first, second, and third pad switches so as to be open in normal operation and so as to be selectively closed in the test mode.

8. The semiconductor body of claim 1, further comprising:

an input buffer, having an input coupled to the terminal pad and having an output coupled to the core functional logic;

said first switch for selectively connecting the output of the input buffer to the first test terminal.

9. A method of testing output circuitry of an integrated circuit, the output circuitry including an output buffer having an input coupled to core functional circuitry and an output coupled to a terminal pad, comprising the steps of:

disconnecting the input of the output buffer from the core functional circuitry;

connecting the input of the output buffer to a first test terminal;

connecting the output of the output buffer to a second test terminal;

applying a test input signal at a first logic level to the first test terminal, for receipt by the input of the output buffer;

measuring, at the second test terminal, the drive strength of the output buffer in response to the test input signal at the first logic level;

applying a test input signal at a second logic level to the first test terminal, for receipt by the input of the output buffer; and

measuring, at the second test terminal, the drive strength of the output buffer in response to the test input signal at the second logic level.

10. The method of claim 9, wherein the method further comprises:

connecting the output of the output buffer to a load test terminal;

connecting a load to the load test terminal prior to the applying steps;

and wherein the measuring steps each comprise:

measuring a voltage drop across the load to determine a drive current from the output buffer.

11. The method of claim 9, wherein the method further comprises:

connecting the output of the output buffer to the load test terminal;

disabling the output buffer;

applying a varying test voltage to the load test terminal;

measuring the voltage at the second test terminal to determine if the voltage at the output of the output buffer follows the varying test voltage.

12. The method of claim 9, wherein the output buffer has a drive input for receiving a drive signal controlling the drive level of the output buffer;

wherein the integrated circuit further comprises a boundary scan cell connected between the drive input of the output buffer and the core functional logic, for providing the drive signal to the output buffer;

and wherein the method further comprises:

storing a selected drive signal in the boundary scan cell, prior to the applying steps.

13. The method of claim 9, wherein the integrated circuit includes a plurality of output buffers, each associated with one of a plurality of terminal pads, and each of the output buffers also associated with a plurality of control switches, the plurality of control switches comprising, for each of the output buffers, an isolation control switch connected between the core functional circuitry and the input of the output buffer, a first test switch connected between the input of the output buffer and the first test terminal, and a second test switch connected between the output of the output buffer and the second test terminal;

wherein the integrated circuit further comprises a first test pad control switch connected between the first test terminal and each of the first test switches of the plurality of output buffers, and a second

test pad control switch connected between the second test terminal and each of the second test switches of the plurality of output buffers;

and wherein the method further comprises:

prior to the applying step, closing the first and second test pad control switches.

14. The method of claim 9, wherein each measuring step measures a propagation delay between the applying step and a time at which the output buffer drives the second test terminal to a threshold voltage.

15. The method of claim 9, wherein the integrated circuit is disposed on a semiconductor wafer in combination with a plurality of similar integrated circuits;

wherein each of the plurality of integrated circuits includes output circuitry including an output buffer having an input coupled to core functional circuitry and an output coupled to a terminal pad;

and wherein each of the plurality of integrated circuits includes a plurality of control switches, the plurality of control switches comprising an isolation control switch connected between the core functional circuitry and the input of the output buffer, a first test switch connected between the input of the output buffer and the first test terminal, and a second test switch connected between the output of the output buffer and the second test terminal, the first and second test terminals of each of the plurality of integrated circuits being connected together to first and second test bus conductors.

16. An integrated circuit, comprising:

functional circuitry having at least one output;

an output buffer having an input, and having an output coupled to an externally accessible functional terminal of the integrated circuit; and

a first switch for selectably coupling the input of the output buffer to an output of the functional circuitry;

a second switch for selectably coupling the input of the output buffer to an externally accessible test terminal on the integrated circuit; and

control circuitry for closing the first switch and opening the second switch, during functional operation of the integrated circuit.

17. The integrated circuit of claim 16, wherein the control circuitry is also for opening the first switch and closing the second switch, during test operation of the integrated circuit.

18. A method of testing an output buffer on an integrated circuit, comprising the steps of:

isolating an input of the output buffer from functional circuitry on said integrated circuit;

connecting the input of the output buffer to an externally accessible terminal of the integrated circuit;

after the connecting step, applying test signals to the externally accessible terminal of the integrated circuit; and

comparing output signals generated by the output buffer responsive to the applying step to expected signals corresponding to the test signals.

19. A semiconductor body upon which at least one integrated circuit is disposed, said at least one integrated circuit comprising:

functional circuitry having at least one output;

an output buffer having an input, and having an output coupled to an externally accessible functional terminal of the integrated circuit; and

a first switch for selectably coupling the input of the output buffer to an output of the functional circuitry;

a second switch for selectably coupling the input of the output buffer to an externally accessible test terminal on the integrated circuit; and

control circuitry for closing the first switch and opening the second switch, during functional operation of the integrated circuit.

20. The semiconductor body of claim 19, wherein the control circuitry is also for opening the first switch and closing the second switch, during test operation of the integrated circuit.

21. The semiconductor body of claim 19, wherein a plurality of integrated circuits are disposed thereupon;

and wherein each of the plurality of integrated circuits comprises:

functional circuitry having at least one output;

an output buffer having an input, and having an output coupled to an externally accessible functional terminal of the integrated circuit; and

a first switch for selectably coupling the input of the output buffer to an output of the functional circuitry;

a second switch for selectably coupling the input of the output buffer to an externally accessible test terminal on the integrated circuit; and

control circuitry for closing the first switch and opening the second switch, during functional operation of the integrated circuit.

22. The semiconductor body of claim 21, wherein the control circuitry of each of the plurality of integrated circuits is also for opening the first switch and closing the second switch, during test operation of the integrated circuit.

23. A semiconductor body upon which at least one integrated circuit is disposed, said at least one integrated circuit comprising:

functional circuitry having an output;

an output buffer, having an input, and having an output coupled to an externally accessible functional terminal of the integrated circuit;

a first switch for selectably coupling the input of the output buffer to an output of the functional circuitry;

a second switch for selectably coupling the input of the output buffer to a first externally accessible test terminal on the integrated circuit;

a third switch for selectably coupling the output of the output buffer to a second externally accessible test terminal on the integrated circuit; and

control circuitry for closing the first switch and opening the second and third switches, during functional operation of the integrated circuit.

24. The semiconductor body of claim 23, wherein the control circuitry is also for opening the first switch and closing the second and third switches, during test operation of the integrated circuit.

25. The semiconductor body of claim 22, wherein a plurality of integrated circuits are disposed thereupon.

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26. A method of measuring on-resistance of an output buffer of an integrated circuit, the output buffer for driving a functional output terminal of the integrated circuit during functional operation, comprising the steps of:

isolating the functional output terminal;

connecting a first external test terminal to the output of the output buffer;

causing the output buffer to drive its output to a first unloaded voltage level;

measuring the first unloaded voltage level at the first test terminal responsive to the causing step;

connecting a load to the output of the output buffer via a second test terminal;

after the step of connecting a load, measuring a first loaded voltage level at the first test terminal;

after the step of connecting a load, measuring a first current flow through the load; and

determining a first on-resistance of the output buffer from the first measured current flow and the measured first unloaded and first loaded voltage levels.

27. The method of claim 26, wherein the measuring steps are performed using a voltage measurement circuit having a high input impedance, so that the current flow at the first test terminal during the measuring steps is minimal.

28. The method of claim 26, further comprising:

disconnecting the load from the output of the output buffer via the second test terminal;

then causing the output buffer to drive its output to a second unloaded voltage level;

measuring the second unloaded voltage level at the first test terminal responsive to the causing step;

connecting a load to the output of the output buffer via the second test terminal;

after the step of connecting a load, measuring a second loaded voltage level at the first test terminal;

after the step of connecting a load, measuring a second current flow through the load; and

determining a second on-resistance of the output buffer from the second measured current flow and the measured second unloaded and second loaded voltage levels.

29. A method of testing an input buffer on an integrated circuit, the input buffer having an input coupled to an external functional terminal, the method comprising the steps of:

applying a varying voltage to a first external test terminal also coupled to the input of the input buffer; and

monitoring an output of the input buffer at a second external test terminal coupled to the output of the input buffer during the applying of the varying voltage, to detect changes in voltage at the output of the input buffer.

30. A method of testing input circuitry of an integrated circuit, the input circuitry including an input buffer having an input coupled

to a terminal pad and an output coupled to core functional circuitry, comprising the steps of:

connecting the input of the input buffer to a first test terminal;

connecting the output of the input buffer to a second test terminal;

applying a test input signal at a first logic level to the first test terminal, for receipt by the input of the input buffer;

measuring, at the second test terminal, the response of the input buffer to the applying step.

31. The method of claim 30, wherein the applying step comprises:

varying the voltage applied to the first test terminal within an input low level voltage range;

and wherein the measuring step comprises:

monitoring a logic level at the second test terminal to determine whether the logic level remains constant during the varying step;

and further comprising:

varying the voltage applied to the first test terminal within an input high level voltage range; and

monitoring a logic level at the second test terminal to determine whether the logic level remains constant during the step of varying the applied voltage within the input high level voltage range.

32. The method of claim 30, wherein the applying step comprises:

varying the voltage applied to the first test terminal from within a first voltage range to at or beyond a first threshold voltage outside of the first voltage range;

wherein the measuring step comprises:

monitoring a logic level at the second test terminal to determine whether the logic level changed state responsive to the varying step;

and wherein the method further comprises:

responsive to the monitoring step determining that the logic level changed state, again varying the voltage applied to the first test terminal from at or beyond the first threshold voltage to a second threshold voltage nearer to the first voltage range than the first threshold voltage; and

again monitoring a logic level at the second test terminal to determine whether the logic level changed state responsive to the step of varying the voltage applied to the first test terminal from at or beyond the first threshold voltage to the second threshold voltage.

33. The method of claim 30, wherein the integrated circuit is disposed on a semiconductor wafer in combination with a plurality of similar integrated circuits;

wherein each of the plurality of integrated circuits includes input circuitry including an input buffer having an input coupled to a terminal pad and an output coupled to core functional circuitry;

wherein each of the plurality of integrated circuits includes a plurality of control switches, the plurality of control switches comprising a first test switch connected between the input of the input

buffer and the first test terminal, and a second test switch connected between the output of the input buffer and the second test terminal, the first and second test terminals of each of the plurality of integrated circuits being connected together to first and second test bus conductors.

34. A method of testing for the absence of output drive capability at an output of a first circuit, the output of the first circuit connected to an output of a second circuit, comprising the steps of:

disabling the output of the first circuit;

outputting a varying voltage from the output of the second circuit; and

during the outputting step, monitoring current flow in a connection between the outputs of the first and second circuits.

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